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EXAMINER	
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ART UNIT	PAPER NUMBER
2111	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/706,419	STULTZ, PAUL D.	
	Examiner	Art Unit	
	CHRISTOPHER A. DALEY	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-18,20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

/DETAILED ACTION

1. Claims 1-3, 5-18, 20 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1 – 3, 5-18, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goodman et al (US6282601) hereinafter Goodman in view of Kim (US6938253).

4. As to claim 1, Goodman discloses an information handling system, comprising: a plurality of processors coupled to a processor bus (Goodman teaches in figure 1 of a plurality of processors 12a, 12b ... 12n, COL. 3, Lines 1 - 10)., and a memory (a system memory 16 in figure 1, COL. 3, Lines 1 - 10).

Goodman does not explicitly teach wherein each of the processors is operable to enter an interrupt mode and wherein a uniquely addressable semaphore in memory is associated with each processor and indicates whether the associated processor has exited the interrupt mode.

However, Kim teaches wherein each of the processors is operable to enter an interrupt mode and wherein a uniquely addressable semaphore in memory is associated with each processor and indicates whether the associated processor has

exited the interrupt mode. Kim teaches in figure 2 of a multiple processor system with processors such as 12 and 14. Said processors are coupled to a semaphore manager 22 .Said figure shows a semaphore register 68 that is coupled to both processors 12 , and 14. Register 68 can be set by either processor to gain access to shared resources, COL. 5, lines 32 – 54.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the semaphore system of Kim in the computer system of Goodman to have a means of managing the multiple interrupts in a multi-processor system, COL. 2, lines 32 – 43.

One of ordinary skill in the art would have been motivated to use the semaphore system of Kim in the computer system of Goodman to have a means of managing the multiple interrupts in a multi-processor system, COL. 2, lines 32 – 43);

Kim teaches each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator (the semaphores are stored in control register as illustrated in Figure 3. In the semaphore controller the address of the semaphore is shown. For example, the location of the status is at address 400, set bit request is at 4004, set bit clear is at 4008, COL. 6, lines 54 - 65).

Kim discloses wherein each processor is operable to access the semaphores associated with the processors of the information handling system on a non-exclusive basis (Figure 2 illustrates semaphore register 68 coupled to both processor 12 and processor 14, which have access to said register, COL. 5, lines 45 - 53).

5. As to claim 2, Kim discloses the information handling system, wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator (The semaphores are stored in control register 68 as illustrated in Figure 2 with said offset, COL. 6, lines 30 – 43).

6. As to claim 3, Kim discloses the information handling system, wherein each processor is operable to access the semaphores associated with the processors of the information handling system (Figure 2 illustrated the coupling of both processors to the semaphore register. Further, Figure 3 shows examples of unique semaphores settings, COL. 6, lines 54 - 65).

7. As to claim 5, Goodman discloses the information handling system, wherein the memory location associated with the storage of the semaphores associated with the processors of the information handling system is memory space dedicated to storing data associated with the entry of the processors into interrupt mode (Said memory space allocation for interrupt sequences, such as power-on self test, COL. 4, lines 10 – 18).

8. As to claim 6, Goodman discloses the information handling system, wherein the the interrupt mode is system management interrupt mode (said mode, COL. 3, lines 42 – 45).

9. As to claim 7, Goodman discloses the information handling system, wherein the interrupt mode is a system management interrupt mode (said mode, COL. 3, lines 42 – 45); Wherein the semaphore associated the semaphore associated with a processor is stored in a memory location that is offset from a base memory location by a unique offset indicator associated with said processor (Figure 1 illustrates control register 106 in each processor that has a unique offset, page 1, paragraph 0016); and wherein each processor is operable to access the semaphores associated with the processors of the information handling system on a non-exclusive basis (Each processor has said access via the CAU unit. That arbitrates all semaphore requests, page 1, and paragraph 0016).

10. As to claim 8, Goodman discloses a method for processing an interrupt in a multiple processor computer system, comprising the steps of: for each processor, entering interrupt mode (each processor enters the interrupt mode from the assertion of an SMI interrupt to all processors, COL. 4, Lines 54 - 56)., Kim teaches for each processor, setting a semaphore associated with the processor to indicate that the processor has exited the interrupt mode, wherein a uniquely addressable semaphore in a memory of the computer system is associated with each processor (Figure 3 illustrates said process COL. 6, lines 43 - 53); and teaches for each non-interrupt handling processors, exiting interrupt mode up following the negation of the semaphore associated with the processor (Figure 3 illustrates how the exit phase is accomplished by the processor by appropriate bit setting, COL. 6, lines 54 - 65).

Kim discloses wherein each processor is operable to access the semaphores associated with the processors of the information handling system on a non-exclusive basis (Figure 2 illustrates semaphore register 68 coupled to both processor 12 and processor 14, which have access to said register, COL. 5, lines 45 - 53).

11. As to claim 9, Kim discloses the method for processing an interrupt in a multiple processor computer system, wherein the step of setting a semaphore for each processor comprises the step of setting the semaphore for each processor on a non-exclusive basis (Figure 2 illustrates said method, COL. 5, lines 45 - 57).

12. As to claim 10, Kim discloses the method for processing an interrupt in a multiple processor computer system, wherein the step of negating the semaphores of the non-interrupt handling processors of the computer system comprises the step of negating the semaphores of the non-interrupt handling processors of the computer system on a non-exclusive basis (Figure 2, with semaphore register 68 can be set by either processor, COL. 5, lines 45 - 55).

13. As to claim 11, Goodman discloses the method for processing an interrupt in a multiple processor computer system, wherein the interrupt is a system management interrupt (the interrupt mode is said mode, COL. 3, lines 42 - 45).

14. As to claim 12, Kim discloses the method for processing an interrupt in a

multiple processor computer system, wherein each of the semaphores are stored in a memory location that is offset from a base memory location by a unique offset indicator (Figure 3 illustrates content of storage device ,with semaphore bits shown, COL. 6, lines 44 - 53).

15. As to claim 13, Kim discloses the method for processing an interrupt in a multiple processor computer system, wherein the step of setting a semaphore for each processor comprises the step of setting the semaphore for each processor on a non-exclusive basis (Figure 3 shows samples of setting semaphore bits, COL. 6, lines 54 - 59);
wherein the step of negating the semaphores of the non-interrupt handling processors of the computer system comprises the step of negating the semaphores of the non-interrupt handling processors of the computer system on a non-exclusive basis (Figure 2, COL. 6, lines 16 - 43); and
wherein each of the semaphores are stored in a memory location that is offset from a base memory location by a unique offset indicator (Figure 3 , illustrating address with offset of the location of the semaphores, such as 4000, 4004, etc).

16. As to claim 14, Goodman discloses the method for processing an interrupt in a multiple processor computer system, wherein the interrupt is a system management interrupt (Goodman teaches of the interrupt mode is said mode, COL. 3, lines 42 - 45),

Kim teaches wherein the step of setting a semaphore for each processor comprises the step of setting the semaphore for each processor on a non-exclusive basis; wherein the step of negating the semaphores of the non-interrupt handling processors of the computer system comprises the step of negating the semaphores of the non-interrupt handling processors of the computer system on a non-exclusive basis (Figure 2 illustrates the manipulation of semaphore for each processors COL. 6, lines 16 - 53).

17. As to claim 15, Goodman discloses a computer system, comprising'. a plurality of processors, a memory (figure 1 of a plurality of processors 12a, 12b ... 12n, COL. 3, lines 1 - 10);

a memory (a system memory 16 in figure 1, COL. 3, lines 1 - 10),.

wherein the architecture of the processors and the memory is a non-uniform memory access architecture (the support other multiple computer systems comprising numa architecture machines, COL. 2, lines 55 - 67); and

Kim teaches wherein each of the processors is operable to enter an interrupt mode and wherein a uniquely addressable semaphore in memory is associated with each processor and indicates whether the associated processor has exited the interrupt Mode (Kim teaches in figure 2 of a multiple processor system with processors such as 12 and 14. Said processors are coupled to a semaphore manager 22 which comprises semaphore register 68 that can be uniquely addressed, as shown in Figure 3, COL. 3, lines 7 - 26).

Kim discloses wherein each processor is operable to access the semaphores associated with the processors of the information handling system on a non-exclusive basis (Figure 2 illustrates semaphore register 68 coupled to both processor 12 and processor 14, which have access to said register, COL. 5, lines 45 - 53).

18. As to claim 16, Goodman discloses the computer system, wherein the interrupt mode is associated with a system management interrupt (the interrupt mode is said mode, COL. 3, lines 42 - 45).

19. As to claim 17, Kim discloses the computer system, wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator (The semaphores are stored in control register as illustrated in Figure 3 with said offset shown in the address field).

20. As to claim 18, Goodman discloses the computer system, wherein the memory location associated with the storage of the semaphores is memory space dedicated to storing data associated with the entry of the processors into interrupt mode (said memory space allocation for interrupt sequences, such as power-on self test, COL. 4, lines 10 - 18).

21. As to claim 19, Kim discloses the computer system, wherein the semaphores may be accessed by each of the processors on a non-exclusive basis (figure 2 illustrates said multiple semaphore transaction, page 1, paragraph 0008).

22. As to claim 20, Kim discloses the computer system, wherein each of the semaphores is stored in a memory location that is offset from a base memory location by a unique offset indicator (The semaphores are stored in control register as illustrated in Figure 2 with said offset, COL. 6, lines 30 – 43).

Response to Arguments

23. Applicant's arguments filed 2/27/2009 have been fully considered but they are not persuasive. The Applicant has argued that "

The combination of Goodman and Kim fails to teach or suggest all the claim limitations of independent claims 1, 8 and 15. Specifically, the combination fails to teach or suggest that "wherein each processor is operable to access each of the semaphores associated with the processors of the information handling system on a non-exclusive basis," as required by claims 1 and 8, and as similarly required by claim 15. As disclosed in the specification of the present application, a "processor's semaphore may be read or reset by any other processor." (Pub. Spec. at ¶ 22.) To address this limitation, the Examiner relies on Kim. (E.g., Office Action at 3.) The Examiner states that Kim discloses "[m]ultiple processors with multiple semaphore being. simultaneously transacted." (Id.) Applicants find the phrase "simultaneously transacted" to be unclear.

Applicants assume the Examiner is equating the mailboxes found in Kim with the "semaphores" of claim 1. Claim 1 requires that the semaphores indicate "whether the associated processor has exited the interrupt mode." In contrast, the mailboxes of Kim actually contain a process message (Kim 6:18) and "generate a hardware interrupt signal when the respective mailboxes 70a, 70b are 'full'" (Kim 6:16-18)."

In response, the Examiner points to the teaching of Kim in Figures 1, and 2.

Figure 1 illustrates a system comprising of a plurality of processors such as 12 and 14 with a semaphore processing element 22. Said semaphore element provides access to shared resources such as memory elements 26, and 32, along with peripheral devices such as USB 40. Figure 2 details semaphore system with semaphore register 68 is shared register between processor 12 and processor 14. The semaphore register 68 establish who has access to the resource as seen in Figure 3, COL. 5, lines 45 – 57. The simultaneous transaction refers to the capability of using the same resource simultaneously, COL. 5, lines 32 - 44. Mailboxes 70a and 70b are just message boxes indicated status of shared resources, COL. 5, line 45 – COL. 6, line 15. Figure 3 illustrates the contents of the semaphore register, which is illustrated as a 32 bit register, but can be any size, COL. 6, line 44 – 53. Thus applicant's argument is not considered persuasive towards patentability.

Further, the Applicant has argued that "Moreover, Kim does not discuss each of the .semaphores being accessible by each of the processors on a non-exclusive basis. Rather, the processors of Kim clear the task message from the mailboxes associated with each processor. (Kim 6:8-9; 6-26-33.) The processors then send signals to each

other to notify each other that the mailbox is empty. (Kim 6:26-33.) Thus, the mailboxes of Kim are not "accessible by each of the processors" as required by claim 1. Therefore, for at least these reasons, Kim does not disclose the above referenced limitations."

In response, the Examiner points to the teaching of Kim as illustrated in Figure 2. In said Figure, semaphore register 68 is accessed on a non-exclusive basis by either processor 12 or 14, COL. 5, lines 45 – 53. Therefore, the examiner cannot allow the claim, since the prior art discloses the element.

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTOPHER A. DALEY whose telephone number is (571)272-3625. The examiner can normally be reached on 9 am. - 4p m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571 272 3632. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christopher A Daley/
Examiner, Art Unit 2111

/Khanh Dang/
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